# Digital Verification using SV and UVM

# Assignment-4

# Name: Fares Khalaf Sultan

# Q1) ) ALSU

# Package class:

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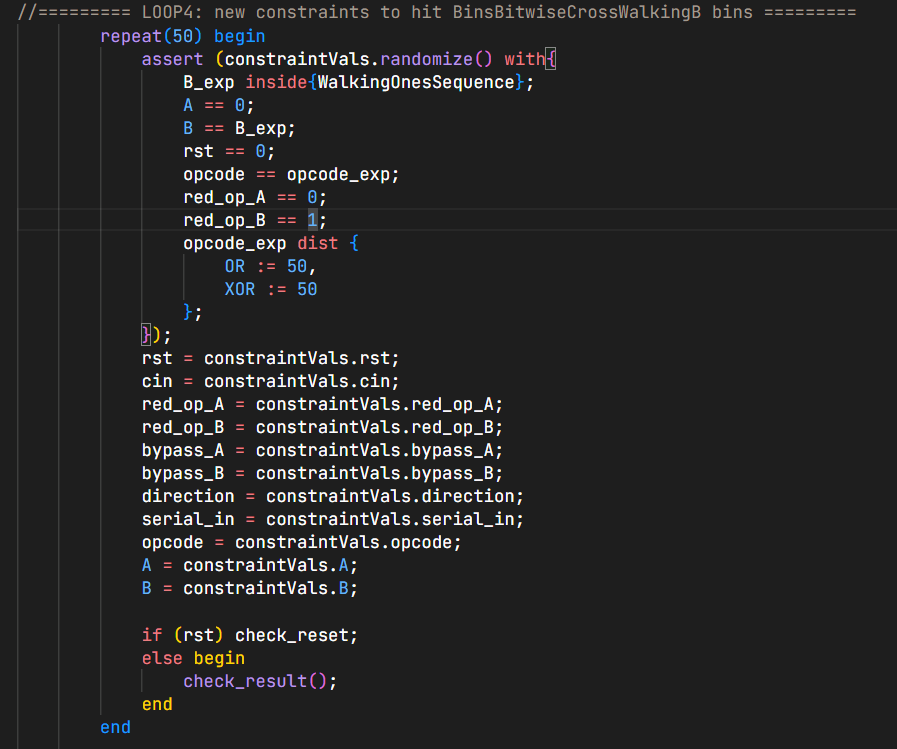
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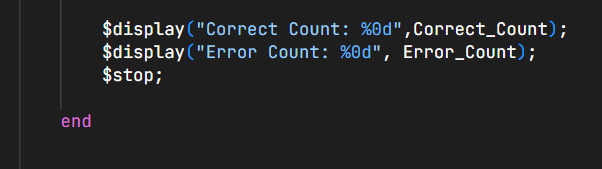
# TestBench:

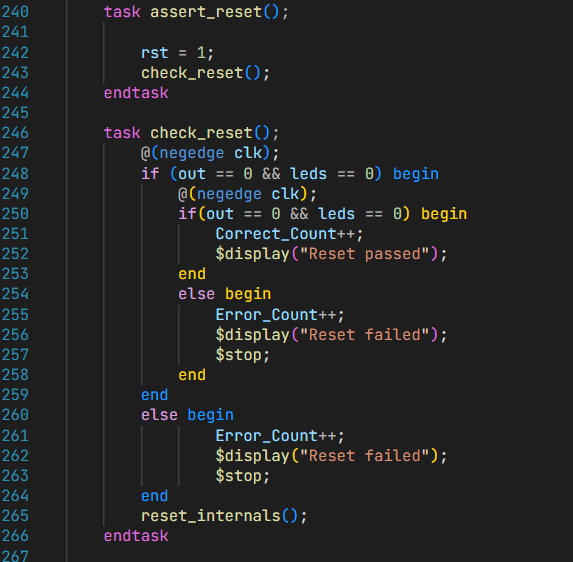
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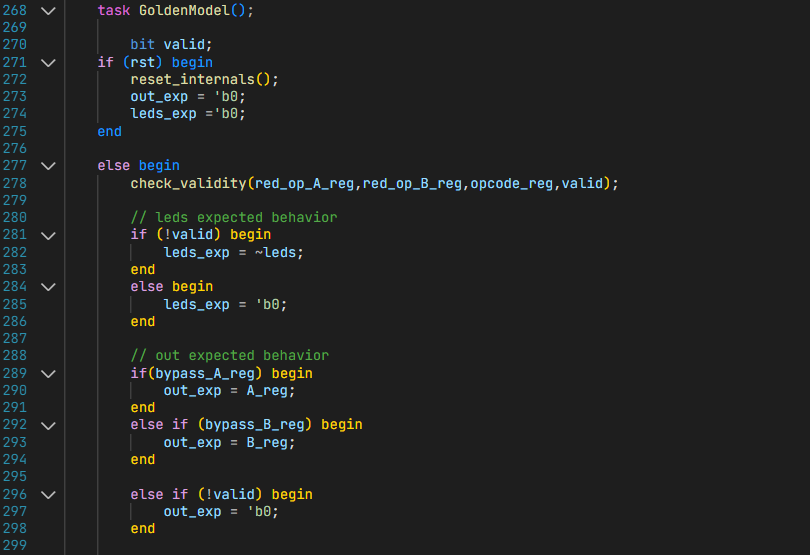
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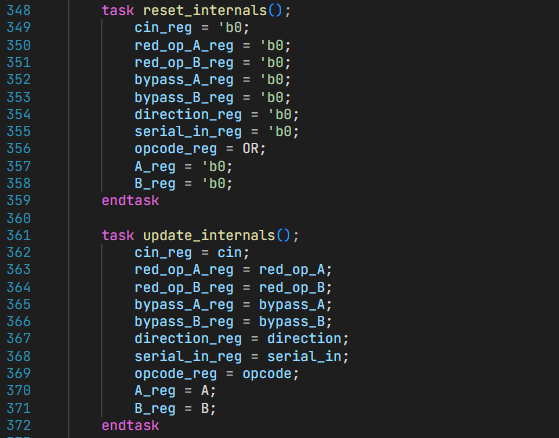
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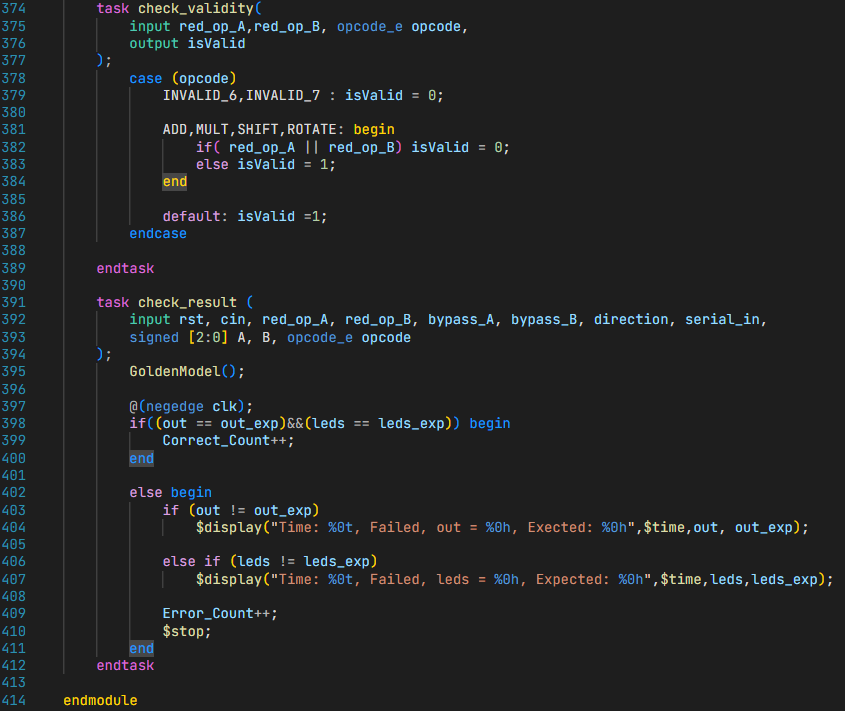












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# Do file:

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# Results:

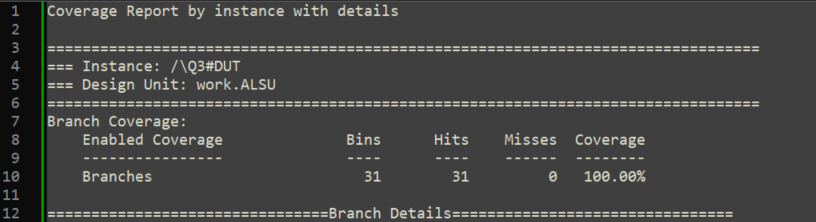
# 

# Waveform:

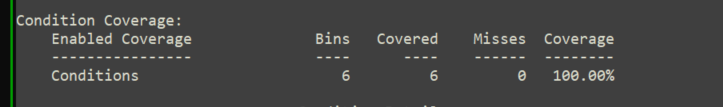
# Functional Coverage Report:

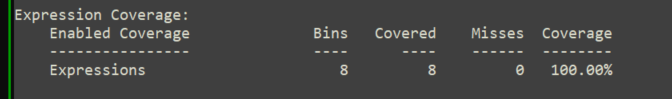
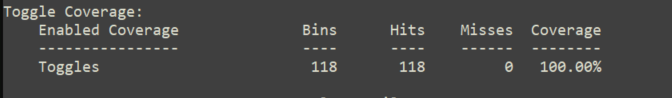
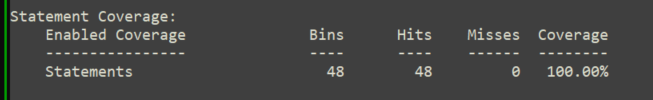
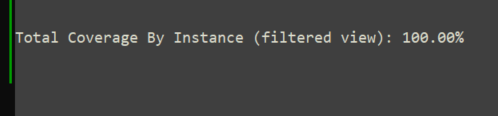
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# Coverage Report:



* Excluded **all False case** in the case statement, since invalid opcodes are handled by the flag (**invalid\_opcode**)





# Q2) Write Assertions:

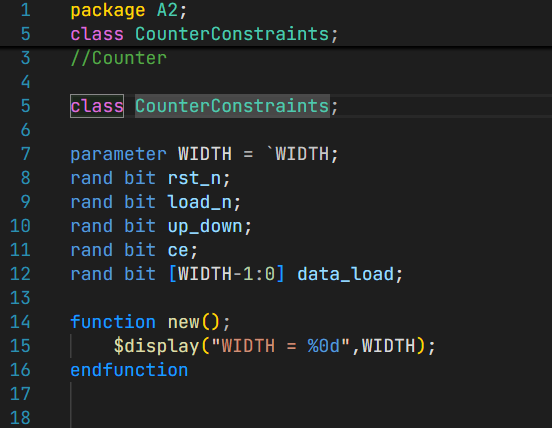
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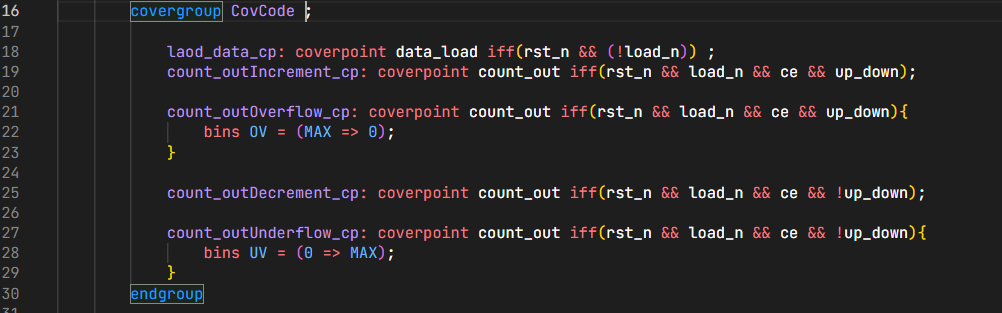
# Q3) Counter:

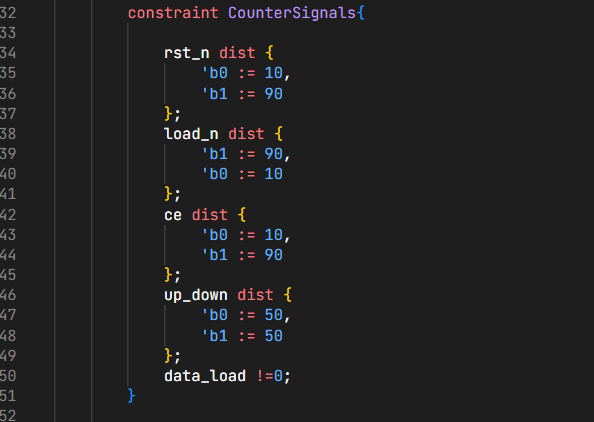
# Verification Plan:

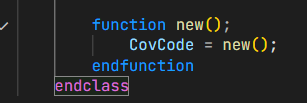
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Label** | **Design Requirement Description** | **Stimulus Generation** | **Functional Coverage** | **Functionality Check** |
| Counter1 | When reset is asserted, Output should be low, and **zero** should be high | Directed at the start of the simulation, then randomized with a constraint to be inactive 90% of the time during the simulation | - | Immediate assertion to verify Async reset functionality, concurrent assertion to check ZERO functionality |
| Counter2 | When **load\_n** is low, **count\_out** should take the value of **load\_data** input | Randomization with constraint on **load\_n** to be high 70% of simulation time | Cover all values of load\_data | Concurrent assertion to check the load\_data |
| Counter3 | Counter should only increment or decrement if **rst\_n** is inactive and, **ce** signal is high, else keep the current **count\_out** value. | Randomization with constraint on **ce** to be high 70% of simulation time | Cover all values of count\_out& transition bin from max to zero | Concurrent assertion to check the count\_out freeze |
| Counter4 | If rst\_n is disabled and ce is enabled, if: **up\_down = o → decrement**  **Up\_down = 1 → increment** | Randomization with constraint on **up\_down** to be high 50% of simulation time | Bin for decrement & another for increment | 2 Concurrent assertions to check the decrement and increment functionalities |
| Counter5 | Check that when the bus **count\_out** value equals the max possible value, **max\_count** should be high | Randomized with no constraints | Bin for max\_count | Concurrent assertion to check the max\_count functionality |

# Constraints class:









# SVA module:

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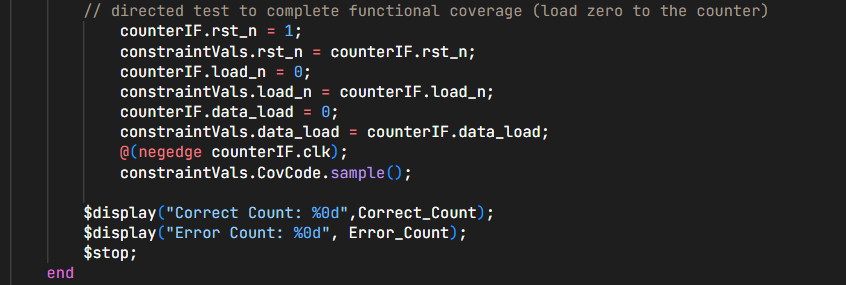
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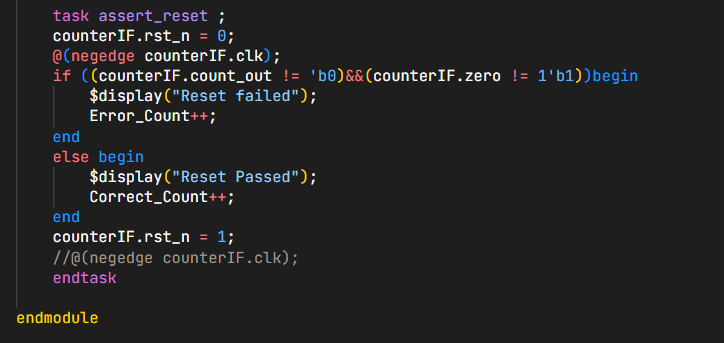
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# Counter interface:

# Top module:

# Test bench:



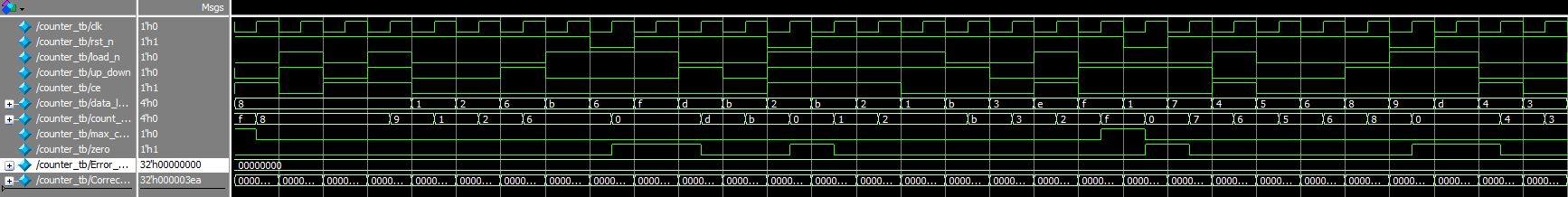


# Do file:

# 

# Result:

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Waveform:

# Functional Coverage:

# 

# Assertion coverage:

# 

# Code Coverage :

# 

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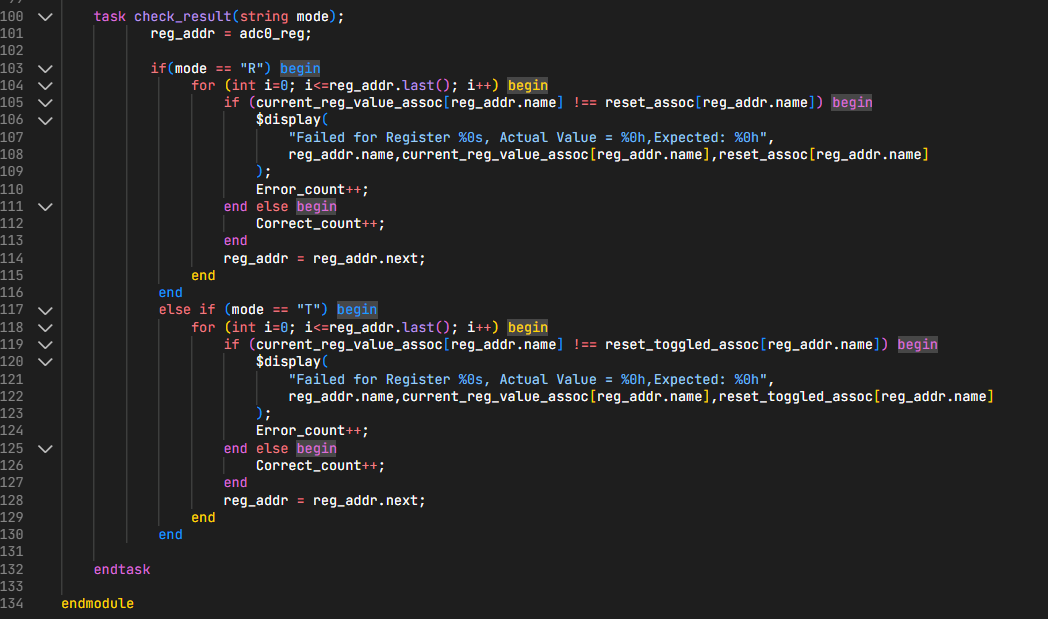
# Q4) Configuration Register:

# Verification Plan:

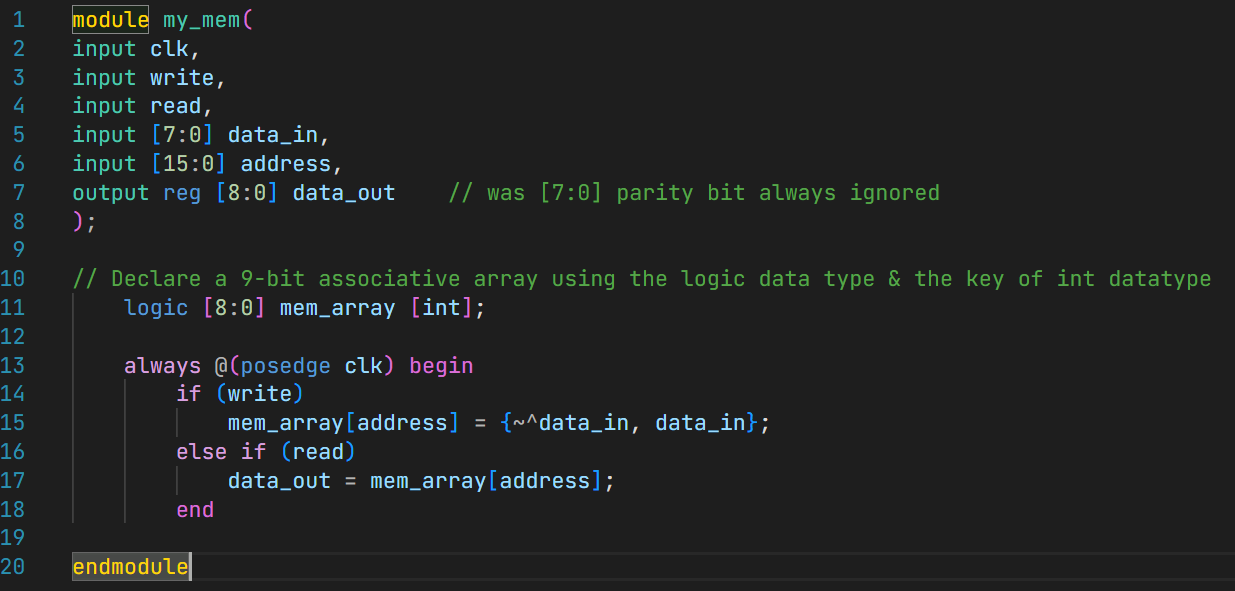
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Label** | **Design Requirement Description** | **Stimulus Generation** | **Functional Coverage** | **Functionality Check** |
| Config1 | Check reset functionality by asserting reset and compare each register value to its corresponding in reset\_assoc[] array. | Directed at the start of the simulation | - | A checker in the testbench to ensure correct reset values for every register |
| config2 | For each register, write the inverted value for its default reset value, so that any unwritable bit is detected | Directed during the simulation | **-** | A checker in the testbench to ensure correct values for every register |

# TestBench:

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# Fixed Design:



# Do file:

# Results:

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# Bug:

|  |  |  |  |
| --- | --- | --- | --- |
| **Resigter** | **Stimulus** | **Expected output** | **Actual output** |
| Adc0\_reg | Toggled reset default value | ‘h0000 | ‘hFFFE |
| Adc1\_reg | Toggled reset default value | ‘hFFFF | ‘hFEFF |
| Temp\_sensor0\_reg | Toggled reset default value | ‘hFFFF | ‘hFFFC |
| Temp\_sensor0\_reg | Toggled reset default value | ‘hFFFF | ‘hFFFE |
| analog\_test | reset default value | ‘hABCD | ‘hABCC |
| digital\_test | Toggled reset default value | ‘hFFFF | ‘hFFFE |
| amp\_gain | Toggled reset default value | ‘hFFFF | ‘hFFFE |
| digital\_config | Toggled reset default value | ‘hFFFE | ‘h7FFe |